IN THE CLAIMS:

CLAIMS

Please cancel claims 3, 21, 36.

Please amend the claims as follows:

1. ~~(Once Amended)~~ An interface to transfer data directly between a first hub and a second hub within a computer system, comprising:

a data signal path to transmit data in packets via split transactions; and

a set of command signals, wherein said interface provides a point-to-point connection between said first hub and said second hub, exclusive of an external bus connected directly to the interface.

3. (Cancled)

19. ~~(Once Amended)~~ An interface to transfer data directly between a first hub and a second hub within a computer system, comprising:

a first means for transmitting data between said first hub and said second hub in packets via split transactions; and

a second means for transmitting command signals, wherein said interface provides a point-to-point connection between said first hub and said second hub, exclusive of an external bus connected directly to the interface.

21. (Canceled)

35. ~~(Once Amended)~~ An interface to transfer data between a first hub and a second hub within a computer system, comprising:

a set of data signals and a pair of source synchronous strobe signals, said data signals transmit data in packets via split transactions, said packets including a request

packet and completion packet, said request packet including a transaction descriptor; and

a set of command signals including unidirectional arbitration signal and a common clock signal, wherein said interface provides a point-to-point connection between said first hub and said second hub, exclusive of an external bus connected directly to the point-to-point connection.

36. (Canceled)

37. An interface to transfer data between a memory controller hub and an input/output (I/O) hub of a chipset within a computer system, comprising:

a bi-directional data signal path and a pair of source synchronous strobe signals, said data signal path transmits data in packets via split transactions, said packets including a request packet and completion packet, said request packet including a transaction descriptor ; and

a set of command signals including unidirectional arbitration signal, a bi-directional stop signal, a system reset signal, a common clock signal, and a voltage reference signal.